Electronic Version

Stylesheet Version v1.1.1

Address Error Detection by Merging a Polynomial-Based CRC Code of Address bits with Two Nibbles of Data or Data ECC Bits

Abstract

A memory system provides data error detection and correction and address error detection. A Single-byte Error-Correcting / Double-byte Error-Detecting (SbEC/DbED) code with the byte being a 4-bit nibble is used to detect up to 8-bit errors and correct data errors of 4 bits or less. Rather than generating address parity, which is poor at detecting even numbers of errors, a cyclical-redundancy-check (CRC) code generates address check bits. A 32-bit address is compressed to just 4 address check bits using the CRC code. The 4 address check bits are merged (XOR'ed) with two 4-bit nibbles of the data SbEC/DbED code to generate a merged ECC codeword that is stored in memory. An address error causes a 2-nibble mis-match due to the redundant merging of the 4 address check bits with 2 nibbles of data correction code. The CRC code is ideal for detecting even numbers of errors com-

mon with multiplexed-address DRAMs.